

U.S. Department of Commerce, Patent and Trademark Office				Attorney Docket No.: 026-0044	
				Application No.: 10/813,837	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicant(s): Garlapati et al.	
				Filing Date: March 31, 2004	
				Group Art Unit: 2819	
				Date Submitted: July 14, 2004	

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U.S. Patent Documents				
* Examiner Initial	Document Number	Date	Name	
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Document	Date	Country	Translation		
			Yes	No	
AL JP 1292411 (English abstract)	Nov. 24, 1989	Japan			

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A	AM	Allen et al., "Current and Voltage References," <u>CMOS Analog Circuit Design</u> , 1987, pp. 240-252.
A	AN	Allen et al., "CMOS Analog Circuits and Systems," <u>CMOS Analog Circuit Design</u> , 1987, pp. 589-599.
A	AO	Banba et al., "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," <u>IEEE Journal of Solid-State Circuits</u> , Vol. 34, No. 5, May, 1999, pp. 670-674.

Examiner <i>fg-car</i>	Date Considered 6/30/06
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents						
*Examiner Initial		Document Number	Date	Name		
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		Document	Date	Country	Yes	No
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A	AU	Gray et al., "Band-Gap-Referenced Biasing Circuits," <u>Analysis and Design of Analog Integrated Circuits</u> , Third Edition, 1993, pp. 338-346.				
A	AV	Lee, "Bandgap References in CMOS Technology," <u>The Design of CMOS Radio-Frequency Integrated Circuits</u> , 1998, pp. 233-235.				
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Examiner		Date Considered				
R. J. Lee		6/30/06				
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PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 026-0044
	Application No.: 10/813,837
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Akhil K. Garlapati
	Filing Date: March 31, 2004
	Group Art Unit: 2838
	Examiner Name: Patel, Rajnikant B.
Sheet 1 of 1	Date Submitted: January 30, 2006

U.S. PATENT DOCUMENTS						
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Examiner Signature	[Signature]			Date Considered	6/30/96	

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